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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
CHEN, DAVID Z	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,717	ROOZEBOOM ET AL.	
	Examiner	Art Unit	
	David Chen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/29/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1, 5-8, 10, 20-23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,030,481 B2 to Chudzik et al. ("Chudzik") in

view of U.S. Patent No. 6,221,769 B1 to Dhong et al. ("Dhong") U.S. Patent Application Publication No. 2001/0005046 A1 to Hsuan et al. ("Hsuan").

As to claim 1, although Chudzik discloses an electronic device comprising a semiconductor substrate (200) having a first side and a second side; a vertical trench capacitor (3010) including a plurality of trenches in which dielectric material (3020) is present between the first (3080) and second (3030) conductive surfaces; and a vertical interconnect (210) that extends through the substrate from the first side to the second side, the vertical interconnect (210) being insulated from the substrate (200) by dielectric material (220) (See Fig. 3c, Column 4, lines 3-54, Column 5, lines 11-28), Chudzik does not specifically disclose wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer.

However, Chudzik does disclose the dielectric material of the vertical trench capacitor (3020) can be silicon nitride and can be deposited by chemical vapor deposition (CVD) (See Column 5, lines 11-16) and the structure of forming the vertical interconnect or via is commonly owned by Dhong (See Column 4, lines 3-17).

Dhong discloses wherein the dielectric material (203) of the vertical interconnect (201) is Si_3N_4 (See Fig. 2, Column 6, lines 11-20). Dhong also discloses wherein the dielectric material (203) is deposited by chemical vapor deposition (CVD). In view of the teaching of Dhong, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material

formed from a single deposition layer because using the same dielectric material while deposited using the same deposition process eliminates additional processing steps and the cost can be lowered.

Further regarding claim 1, the limitation "...formed from a single deposition layer" is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

As to claim 5, Chudzik further discloses wherein contact pads (270) for coupling to an external carrier are present on the second side; a first vertical interconnect (210) is

used for grounding and a second interconnect (410) is used for signal transmission (See Fig. 3c, Fig. 4c, Column 4, lines 3-35, Column 6, lines 13-37).

Further regarding claim 5, the claim limitation "...for coupling to an external carrier are present on the second side", "...used for grounding", and "...used for signal transmission" specifies an intended use or field of use, and is treated as non-limiting since it has been held that in device claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex Parte Masham*, 2 USPQ 2d 1647 (Bd. Pat. App. & Inter. 1987).

As to claim 6, Chudzik further discloses wherein the first (210) and second (410) vertical interconnect are designed so as to form a coaxial structure (See Fig. 4c).

As to claim 7, Chudzik further discloses wherein that an integrated circuit is defined on the second side of the substrate (200) (Column 4, lines 19-35).

As to claim 8, Chudzik further discloses wherein the substrate (200) comprises a high-ohmic zone which is present adjacent to the vertical capacitors (3010) and acts as a protection against parasitic currents (See Column 6, lines 41-67).

Further regarding claim 8, the claim limitation "...acts as a protection against

parasitic currents" specifies an intended use or field of use, and is treated as non-limiting since it has been held that in device claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex Parte Masham*, 2 USPQ 2d 1647 (Bd. Pat. App. & Inter. 1987).

As to claim 10, Chudzik discloses further comprising a semiconductor device (102), which semiconductor device is electrically connected to bond pads (270) present on the first side of the substrate (200) (See Fig. 3c, Column 4, lines 19-35).

As to claim 20, although Chudzik does not specifically disclose wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor are formed by deposition a layer of dielectric material on the substrate and partially etching the deposited layer of the dielectric material, Chudzik does disclose the dielectric material of the vertical trench capacitor (3020) can be silicon nitride and can be deposited by chemical vapor deposition (CVD) (See Column 5, lines 11-16) and the structure of forming the vertical interconnect or via is commonly owned by Dhong (See Column 4, lines 3-17).

Dhong discloses wherein the dielectric material (203) of the vertical interconnect

(201) is Si_3N_4 (See Fig. 2, Column 6, lines 11-20). Dhong also discloses wherein the dielectric material (203) is deposited by chemical vapor deposition (CVD).

In view of the teaching of Dhong, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor formed by deposition a layer of dielectric material on the substrate and partially etching the deposited layer of the dielectric material because using the same dielectric material while deposited using the same deposition process eliminates additional processing steps and the cost can be lowered.

Further regarding claim 20, the limitation "...formed by depositing a layer of dielectric material on the substrate and partially etching the deposited layer of dielectric material" is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing

the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

As to claim 21, although Chudzik does not specifically disclose wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor are identical dielectric material formed from a single deposition layer.

However, Chudzik does disclose the dielectric material of the vertical trench capacitor (3020) can be silicon nitride and can be deposited by chemical vapor deposition (CVD) (See Column 5, lines 11-16) and the structure of forming the vertical interconnect or via is commonly owned by Dhong (See Column 4, lines 3-17).

Dhong discloses wherein the dielectric material (203) of the vertical interconnect (201) is Si_3N_4 (See Fig. 2, Column 6, lines 11-20). Dhong also discloses wherein the dielectric material (203) is deposited by chemical vapor deposition (CVD). In view of the teaching of Dhong, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have identical dielectric material for the vertical interconnect and vertical trench capacitor and formed from a single deposition layer because using the same dielectric material while deposited using the same deposition process eliminates additional processing steps and the cost can be lowered.

Further regarding claim 21, the limitation "...formed from a single deposition layer" is a product-by-process limitation that does not structurally distinguish the claimed

invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

As to claim 22, although Chudzik does not specifically disclose wherein the vertical interconnect is substantially filled with conductive material, the conductive material of the vertical interconnect and the second conductive surface of the vertical trench capacitor being formed from a single deposition layer of conductive material, Chudzik does disclose the conductive material (3030) of the vertical trench capacitor (3020) can be Cu and can be deposited by physical vapor deposition (PVD) (See Column 5, lines 11-22) and the structure of forming the vertical interconnect or via is

commonly owned by Dhong (See Column 4, lines 3-17).

Dhong discloses wherein the conductive material (205) of the vertical interconnect (201) is copper (See Fig. 2, Column 6, lines 11-31). Dhong also discloses wherein the conductive material (205) is deposited by physical vapor deposition (PVD). In view of the teaching of Dhong, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have identical conductive material for the vertical interconnect and vertical trench capacitor and formed from a single deposition layer because using the same conductive material while deposited using the same deposition process eliminates additional processing steps and the cost can be lowered.

Further regarding claim 22, the limitation "...formed from a single deposition layer of conductive material" is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing

the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

As to claim 23, although Chudzik discloses an electronic device comprising: a semiconductor substrate (200) having a first side and a second side; a plurality of trenches (3010) on the first side of the substrate (200), each of the trenches (3010) extending into the substrate (200) from the first side; a conductive material (3030) lining each of the trenches (3010); a vertical interconnect (210) that extends through the substrate (200) from the first side to the second side, the vertical interconnect (210) having walls; (See Fig. 3c, Fig. 4c, Column 4, lines 3-54, Column 5, lines 11-28), Chudzik does not specifically disclose a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect.

However, Chudzik does disclose the dielectric material of the vertical trench capacitor (3020) can be silicon nitride and can be deposited by chemical vapor deposition (CVD) (See Column 5, lines 11-16) and the structure of forming the vertical interconnect or via is commonly owned by Dhong (See Column 4, lines 3-17).

Dhong discloses wherein the dielectric material (203) of the vertical interconnect (201) is Si_3N_4 (See Fig. 2, Column 6, lines 11-20). Dhong also discloses wherein the dielectric material (203) is deposited by chemical vapor deposition (CVD). In view of the

teaching of Dhong, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer because using the same dielectric material while deposited using the same deposition process eliminates additional processing steps and the cost can be lowered.

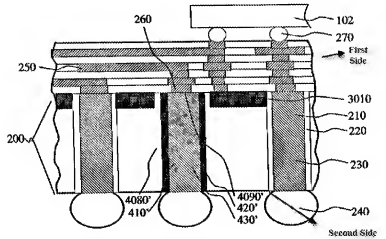
Further regarding claim 23, the limitation "...a single deposition layer..." is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276,

279, 162 USPQ 221, 223 (CCPA 1979).

As to claim 27, Chudzik further discloses wherein the plurality of trenches form a vertical trench capacitor (3010) (See Fig. 3c, Fig. 4c, Column 4, lines 3-54, Column 5, lines 11-28).

Figure 4c



2. Claims 2-4 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,030,481 B2 to Chudzik et al. ("Chudzik") and U.S. Patent No. 6,221,769 B1 to Dhong et al. ("Dhong") as applied to claims 1 and 23 above, and further in view of U.S. Patent Application Publication No. 2001/0005046 A1 to Hsuan et al. ("Hsuan"). The teachings of Chudzik and Dhong have been discussed above.

As to claim 2, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the vertical interconnect has a first part and a second part, which the first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape.

However, Hsuan does disclose wherein the vertical interconnect (44a, 46, 42, 56, 58) has a first part (42) and a second part (56), which the first part is exposed on the first side of the substrate (48a), is narrower than the second part (56) and has a substantially cylindrical shape (See Fig. 2H, ¶ 0030, ¶ 0031, ¶ 0032, ¶ 0035).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the vertical interconnect that has a first part and a second part, which the first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape because this particular structure allows the interconnects to shorten their distance so that signal transmitting path is reduced. By reducing the signal transmitting path, the transmission rate increases so the device performance increases as a result. This particular structure also allows the electro pad or conductive bump to form in the groove or the wider part so that the package size is reduced (See Fig. 2H, ¶ 0047, ¶ 0048).

As to claim 3, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the vertical interconnect includes a plurality of parallel trenches each of which is substantially filled with electrically conductive material.

However, Hsuan does disclose wherein the vertical interconnect includes a plurality of parallel trenches (42) each of which is substantially filled with electrically conductive material (See Fig. 2H, ¶ 0029).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the vertical interconnect with a plurality of parallel trenches each of which is substantially filled with electrically conductive material so that signal transmission can be improved because of separate and short interconnects. The plurality parallel trenches with conductive material can also be utilized as a heat dissipating mean so that the device does not overheat during operation.

As to claim 4, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the first part of the vertical interconnect comprises a plurality of parallel through-holes that extend from the first side of the substrate to the second part of the vertical interconnect, each of the plurality of parallel through-holes being substantially filled with electrically conductive material.

However, Hsuan does disclose wherein the first part (42) of the vertical interconnect (44a, 46, 42, 56, 58) comprises a plurality of parallel through-holes (42) that extend from the first side of the substrate (48a) to the second part of the vertical interconnect (56), each of the plurality of parallel through-holes (42) being substantially filled with electrically conductive material (See Fig. 2H, ¶ 0029, ¶ 0030, ¶ 0031, ¶ 0032, ¶ 0035).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the vertical interconnect with a plurality of

parallel through-holes each of which is substantially filled with electrically conductive material so that signal transmission can be improved because of separate and short interconnects. The plurality parallel through-holes with conductive material can also be utilized as a heat dissipating mean so that the device does not overheat during operation.

As to claim 24, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the vertical interconnect has a first part and a second part, the first part extending from the first side of the substrate to the second part, the second part extending from the second side of the substrate to the first part and being wider than the first part.

However, Hsuan does disclose wherein the vertical interconnect (44a, 46, 42, 56, 58) has a first part (42) and a second part (56), the first part extending from the first side of the substrate (48a) to the second part (56), the second part (56) extending from the second side of the substrate to the first part and being wider than the first part (See Fig. 2H, ¶ 0030, ¶ 0031, ¶ 0032, ¶ 0035).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the vertical interconnect that has a first part and a second part, the first part extending from the first side of the substrate to the second part, the second part extending from the second side of the substrate to the first part and being wider than the first part because this particular structure allows the interconnects to shorten their distance so that signal transmitting path is reduced. By

reducing the signal transmitting path, the transmission rate increases so the device performance increases as a result. This particular structure also allows the electro pad or conductive bump to form in the groove or the wider part so that the package size is reduced (See Fig. 2H, ¶ 0047, ¶ 0048).

As to claim 25, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the vertical interconnect includes a plurality of parallel trenches.

However, Hsuan does disclose wherein the vertical interconnect includes a plurality of parallel trenches (42) (See Fig. 2H, ¶ 0029).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the vertical interconnect with a plurality of parallel trenches so that signal transmission can be improved because of separate and short interconnects. The plurality parallel trenches can also be utilized as a heat dissipating mean so that the device does not overheat during operation.

As to claim 26, although Chudzik and Dhong disclose a vertical interconnect (210) (See Fig. 3c), Chudzik and Dhong do not disclose wherein the first part of the vertical interconnect includes a plurality of parallel trenches each of which extends from the first side of the substrate to the second part of the vertical interconnect.

However, Hsuan does disclose wherein the first part (42) of the vertical interconnect (44a, 46, 42, 56, 58) includes a plurality of parallel trenches (42) each of which extends from the first side of the substrate (48a) to the second part of the vertical

interconnect (56) (See Fig. 2H, ¶ 0029, ¶ 0030, ¶ 0031, ¶ 0032, ¶ 0035).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Hsuan to form the first part of the vertical interconnect with a plurality of parallel trenches each of which extends from the first side of the substrate to the second part of the vertical interconnect so that signal transmission can be improved because of separate and short interconnects. The plurality parallel trenches can also be utilized as a heat dissipating mean so that the device does not overheat during operation.

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,030,481 B2 to Chudzik et al. ("Chudzik") and U.S. Patent No. 6,221,769 B1 to Dhong et al. ("Dhong") as applied to claim 8 above, and further in view of U.S. Patent No. 5,872,393 to Sakai et al. ("Sakai"). The teachings of Chudzik and Dhong have been discussed above.

As to claim 9, although Chudzik discloses wherein the substrate (200) comprises a high-ohmic zone which is present adjacent to the vertical capacitors (3010) (See Column 6, lines 41-67), Chudzik and Dhong do not disclose further comprising a planar capacitor on the first side of the substrate, the planar capacitor including dielectric material formed from common material of the single deposition layer, and wherein the high-ohmic zone separates the planar capacitor from the vertical trench capacitor.

However, Sakai does disclose a planar capacitor (103y, 102b, 103x) on the first

side of the substrate (100), the planar capacitor (103y, 102b, 103x) including dielectric material (102b Silicon Nitride) formed from common material of the single deposition layer, and wherein the high-ohmic zone separates the planar capacitor from the vertical trench capacitor (See Fig. 3, Column 15, lines 39-61).

In view of the teaching of Sakai, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chudzik and Dhong with the teaching of Sakai to form a planar capacitor on the first side of the substrate, the planar capacitor including dielectric material formed from common material of the single deposition layer because the planar capacitor can serve as a decoupling capacitor to reduce noise in RF device and the common dielectric material allows additional processing steps to be reduced and therefore the cost of manufacturing is lowered as well.

Further regarding claim 9, the limitation "...formed from common material of the single deposition layer" is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. It has been held it has been held that "The Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and

the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3, 9, 22, 23, 25, 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Chen whose telephone number is (571)270-7438. The examiner can normally be reached on Monday-Friday 8:00 AM-4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571)272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815

/D. C./
Examiner, Art Unit 2815